PRODUCT SPECIFICATION FOR LCD MODULE

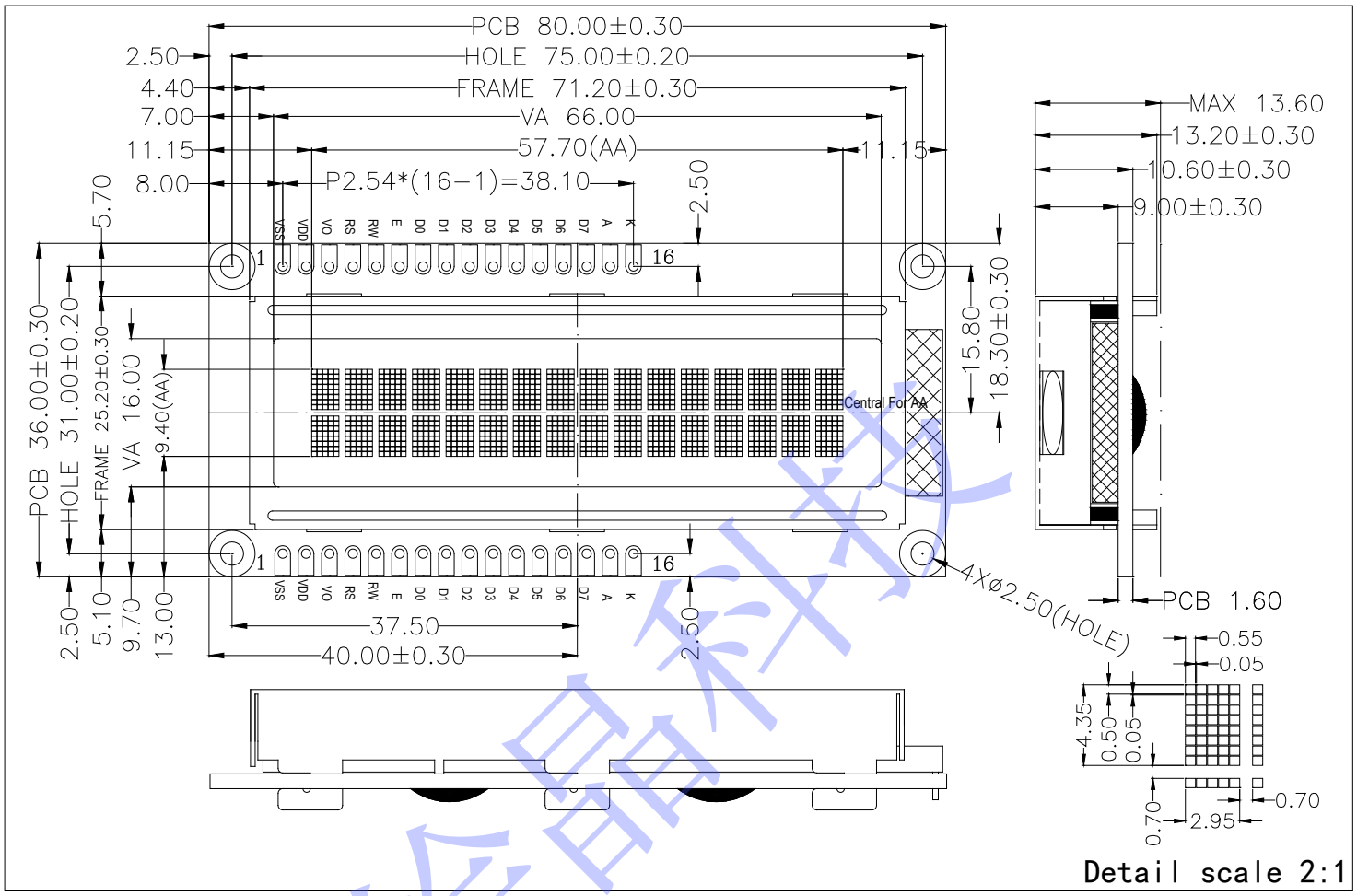
MODULE NO. : 1602ZFV

Customer Approval:

PREPARED BY		DATE	
CHECKED BY		DATE	
APPROVED BY		DATE	

1. Module size

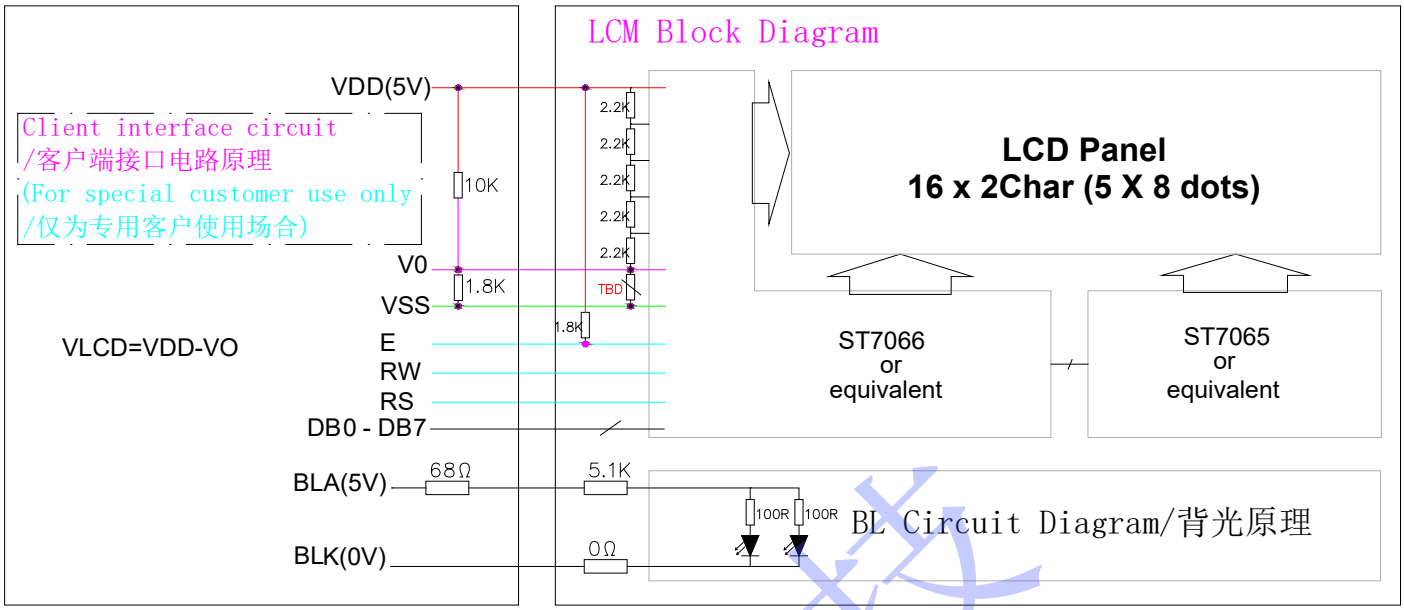
a) 1602ZFV



b) Physical Data

Item	Reference
LCM SIZE (W×h×z)	80.0×36.0×13.2
Viewing area (W×h)	66.0×16.0
Dot spacing (W×h)	0.60×0.55
Dot size (W×h)	0.55×0.50
Character Size	2.95×4.35
Character spacing	3.85×5.05

c) Block Diagram



2. Function introduction

- 5 × 8 dot matrix possible
- Low power operation support:

— 4.75to 5.25V

- Liquid crystal drive waveform

— A (One line frequency AC waveform)

- 4-bit or 8-bit MPU interface enabled
- 80 × 8-bit display RAM (80 characters max.)
- 9,920-bit character generator ROM for a total of 240 character fonts

— 208 character fonts (5 × 8 dot)

— 32 character fonts (5 × 10 dot)

✧ DISPLAY TYPE STN, YELLOW-GREEN, POSITIVE

✧ POLARIZER TRANSFLECTIVE

✧ Applicable LCD duty 1/16 bias 1/5

✧ Operating Temperature -20°C ~ +70°C

✧ Storage Temperature -30°C ~ +80°C

✧ VIEWING DIRECTION 6.0’ CLOCK,

✧ BACKLIGHT: YELLOW-GREEN

✧ Controller ST7066U

✧ If the YOU needs to do other display mode: such as STN Blue TRANSMISSIVE or FSTN POSITIVE TRANSFLECTIVE /如您有需要，也可做其它显示模式：如 STN 蓝膜全透,FSTN 正显半透

3.PIN CONFIGURATIONS

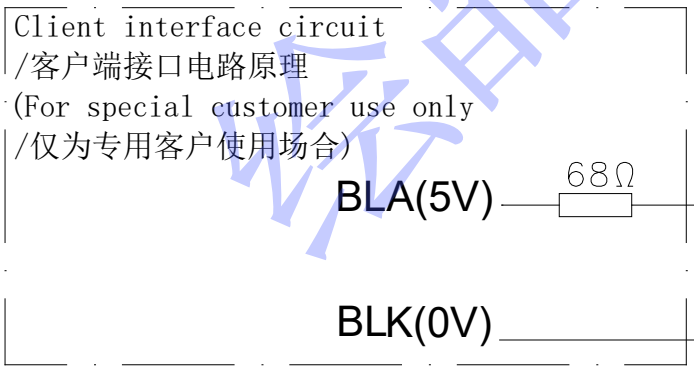
PIN No	Symbol	Level	Function
1	VSS	--	Ground
2	VCC	--	Power supply for logic
3	V0	--	Power supply for VLCD
4	RS	I	=1, Data register (for write and read)
			=0, Instruction register (for write) Busy flag: address counter (for read)
5	RW	I	=0, Write
			=1, Read
6	E	I	Starts data read/write.
7-14	DB0 ~ DB7	I/O	Data Bit0[0:7]
15	LEDA	--	LED Backlight Positive Power Supply
16	LEDK	--	LED Backlight Negative Power Supply

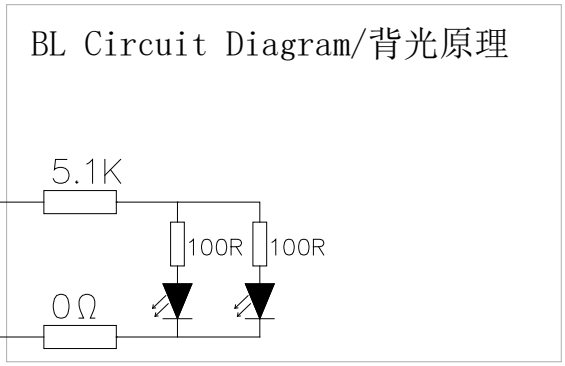
4.ELECTRICAL PARAMETE

4.1 DC Characteristics (TA = 25℃, Vcc = 4.75 V - 5.25 V)

Characteristic	Symbol	Value	Rating			Unit
			Min	Typ	Max	
Operating Voltage	VCC	–	4.75	5.0	5.25	V
LCM Recommend LCD Module Driving Voltage	VLCD	VCC-VO	3.0	4.55	5.25	V
Input High Voltage	VIH	–	0.7VCC	–	VCC+0.3	V
Input Low Voltage	VIL	–	-0.3	–	0.6	V
Output High Voltage	VOH	–	0.7VCC	–	VCC	V
Output Low Voltage	VOL	–	–	–	0.4	V
Operating Current	IDD	=VCC	–	3.66	4.50	MA
Leakage Current (except E signal)	IDO	=VCC	–	–	3.0	uA
Backlight Current	ILED	=VLED(5.0V) (Backlit Voltage)	–	0.45	20	MA
Backlit Voltage	Vbl	VBLA-VBLK	–	5.0	--	V
Backlit Lifetime:	Hour	25℃	50000	--	--	H

Note:voltage tolerance is +/-0.2V whenSuggest theoperatingthetoleranceis +/-0.2V~+/-0.25 it mav affect LCD contrast lighter or deeper.





Note: This backlight application circuit is for special customer applications only/注：此背光应用电路仅为专用客户应用

4.2 Absolute Maximum Ratings

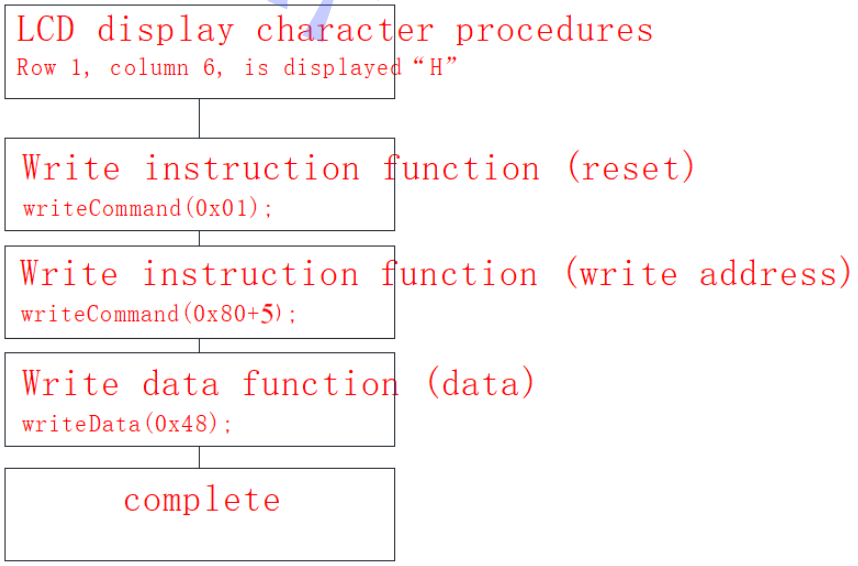
Characteristics	Symbol	Value
Power Supply Voltage	VCC	-0.3 to +7.0
Output High Voltage	VLCD	VCC-10.0 to VCC+0.3
Output Low Voltage	VIN	-0.3 to VCC+0.3

5.Display Data RAM (DDRAM)

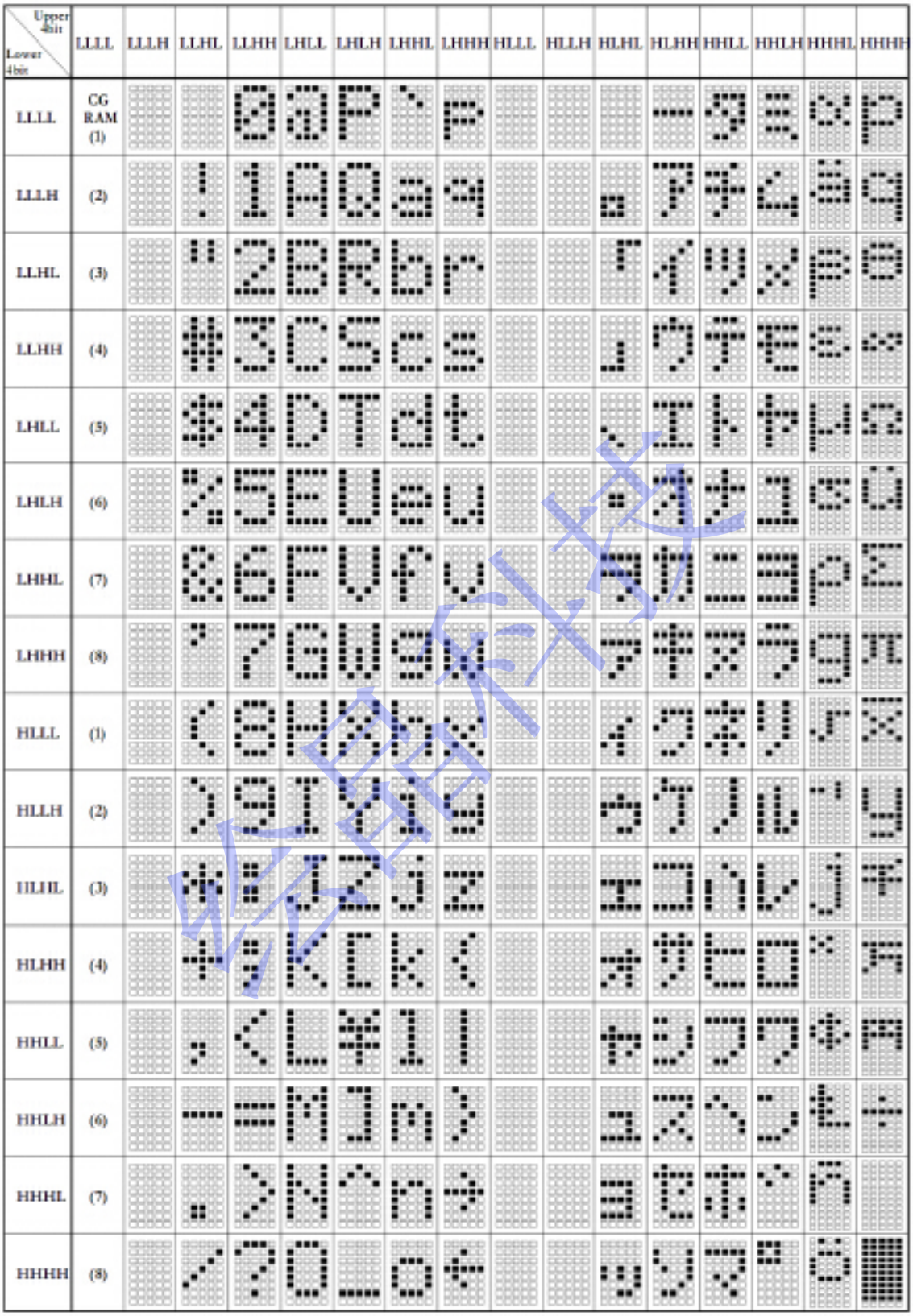
a) DDRAM

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

Write data flow chart



b) Correspondence between Character Codes and Character Patter



c) CGRAM

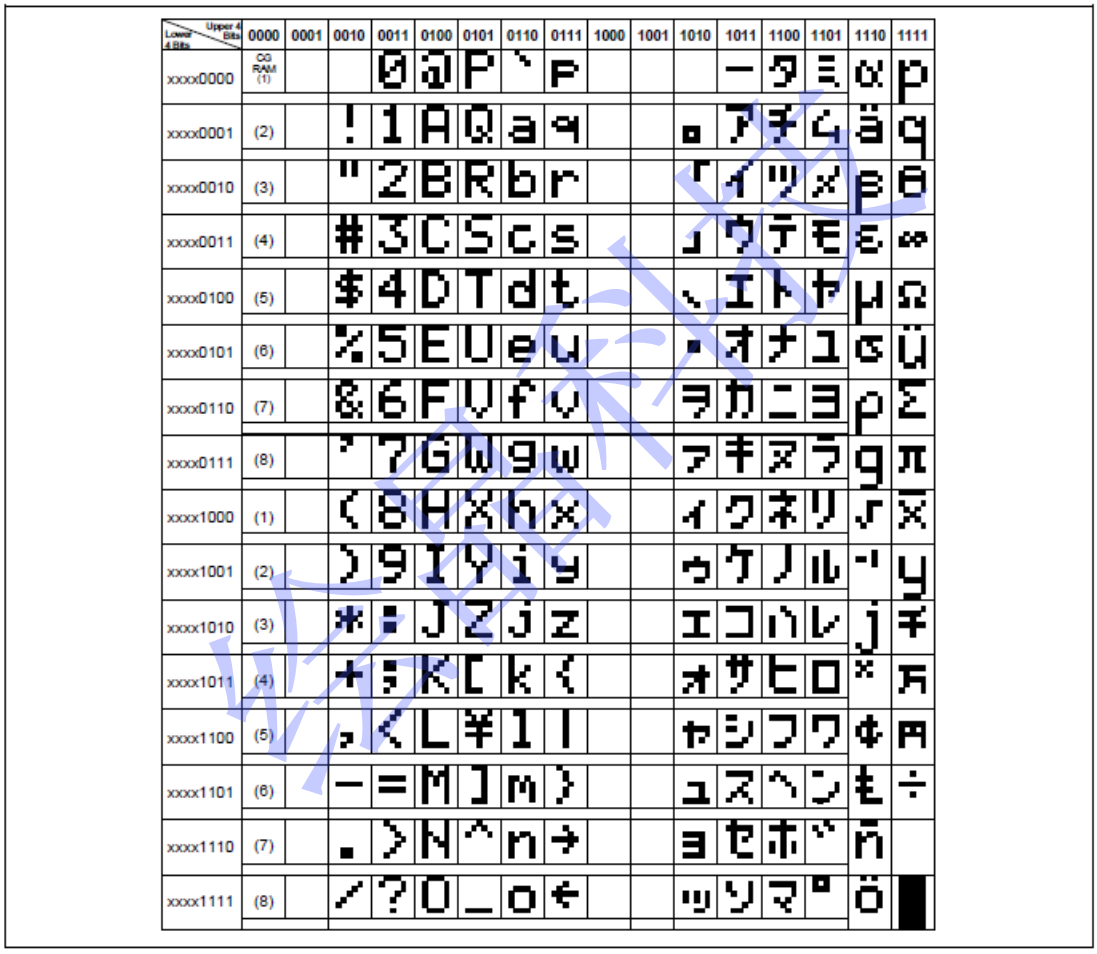
Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 × 8 dots, eight character patterns can be written, and for 5 × 10 dots, four character patterns can be written. Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns.

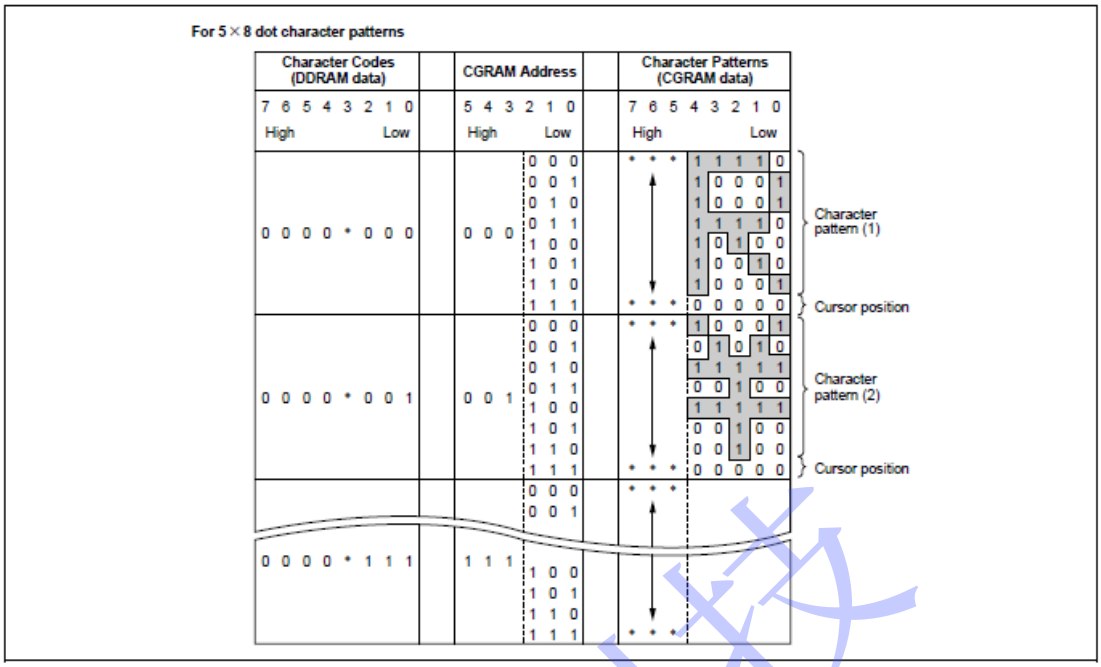
Areas that are not used for display can be used as general data RAM.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A00)



Note: The user can specify any pattern for character-generator RAM.

Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)



Notes: 1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).

2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.

Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.

If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.

3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).

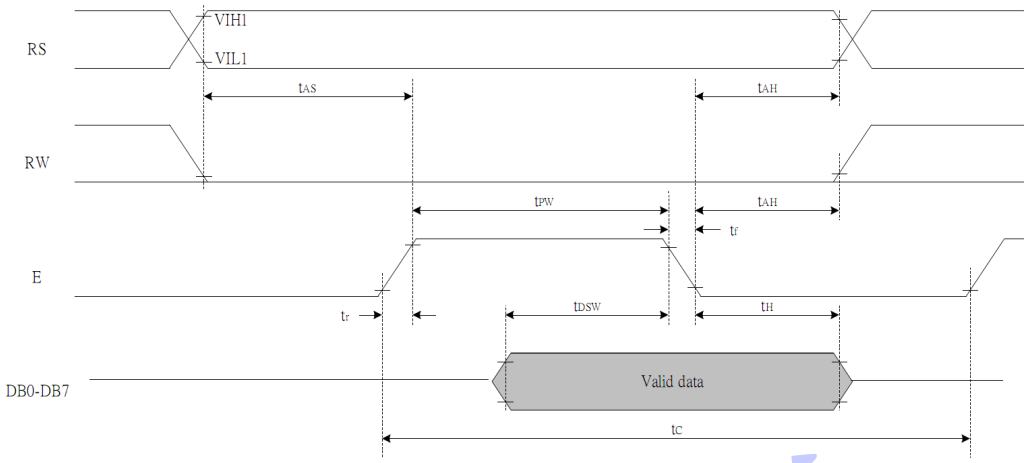
4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.

5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

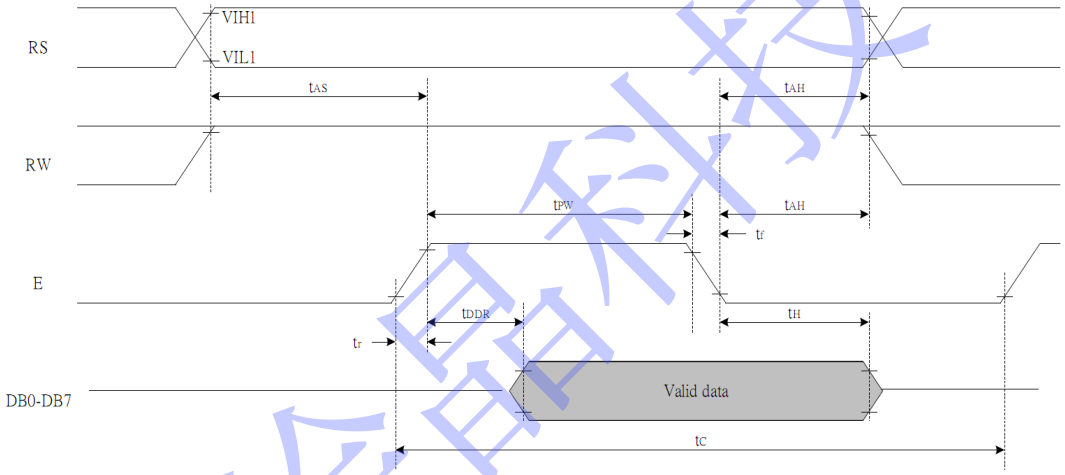
* Indicates no effect.

6.TIMING CHARACTERISTICS

6.1 Writing data from MPU to ST7066U



6.2 Read Operation time



6.3 **AC Characteristics** (TA = 25℃, VCC = 4.75~5.25V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 91KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
t_r, t_f	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to ST7066U)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
t_r, t_f	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from ST7066U to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
t_r, t_f	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	100	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Interface Mode with LCD Driver(ST7065)						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	0	-	2000	ns

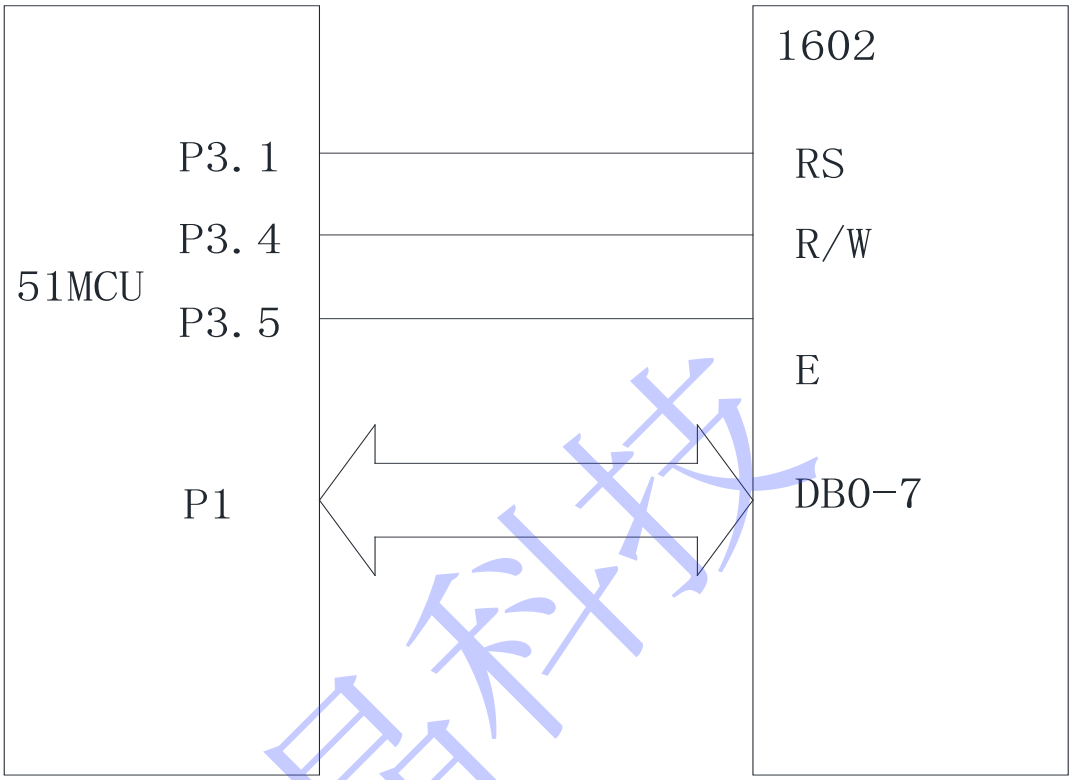
7.Display Control Instruction

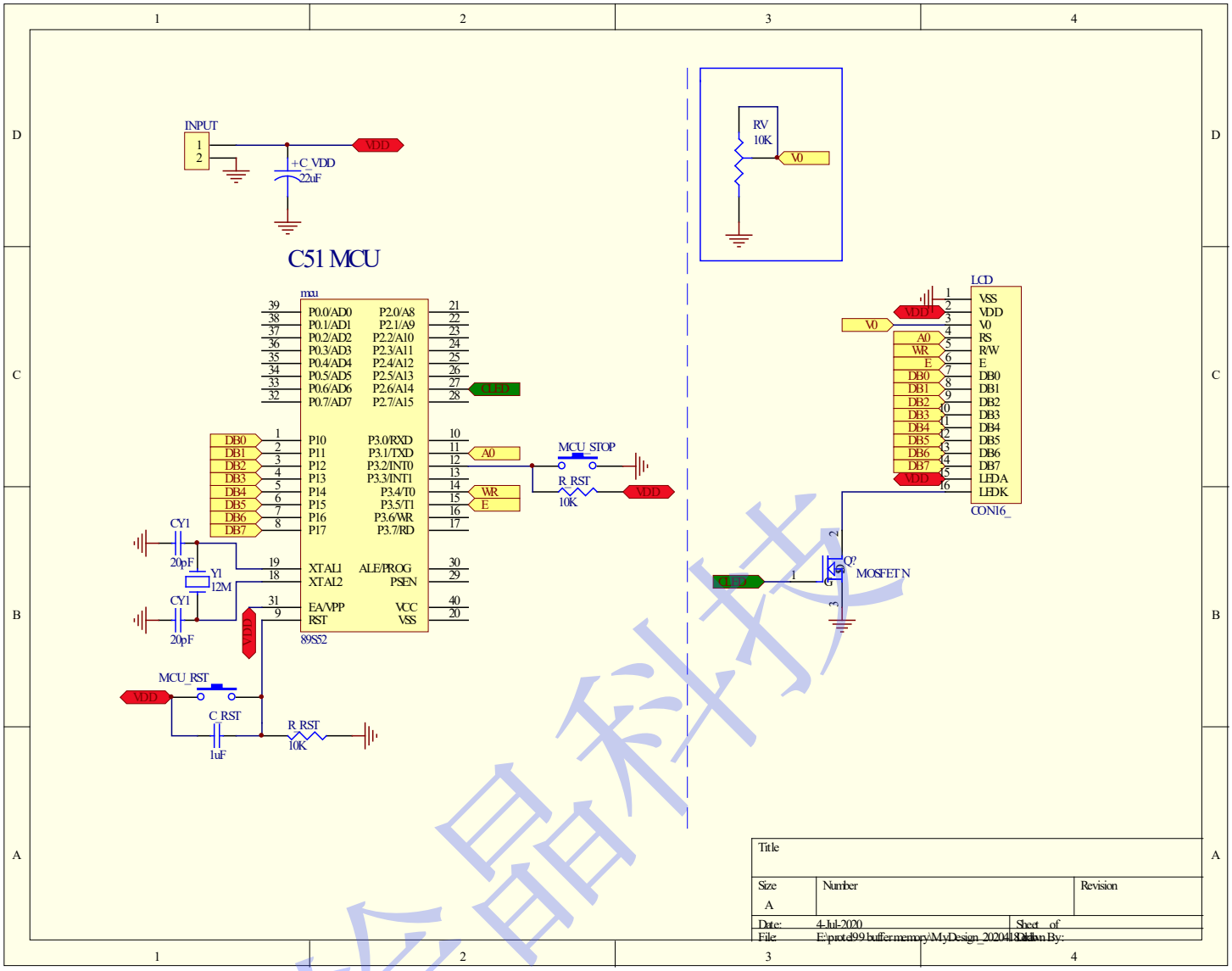
1、Instruction sheet

NO	item	Instruction										HEX	execution time	Operation
		RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0			
1	Clear Display	0	0	0	0	0	0	0	0	0	1	01	1.52ms	Write "20H" to DDRAM and set DDRAM address to "00H" from AC
2	Return Home	0	0	0	0	0	0	0	0	1	0	02	1.52ms	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
3	Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	04	37US	Assign cursor moving direction and enable the shift of entire display
4	Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	08	37US	Set display (D), cursor(C), and blinking of cursor(B) on/off control bit.
5	Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	10	37US	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.
6	Function set	0	0	0	0	1	DL	N	F	-	-	20	37US	DL:interface data is 8/4 bits N:number of line is 2/1 F:font size is 5x11/5x8
7	Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	40	37US	Set CGRAM address in address counter.
8	Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	80	37US	Set DDRAM address in address counter
9	Read Busy Flag and Address Counter	0	0	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		0US	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. ）
10	Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	00	37US	Write data into internal RAM (DDRAM/CGRAM).
11	Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	00	37US	Read data from internal RAM (DDRAM/CGRAM).

“-” don’t care

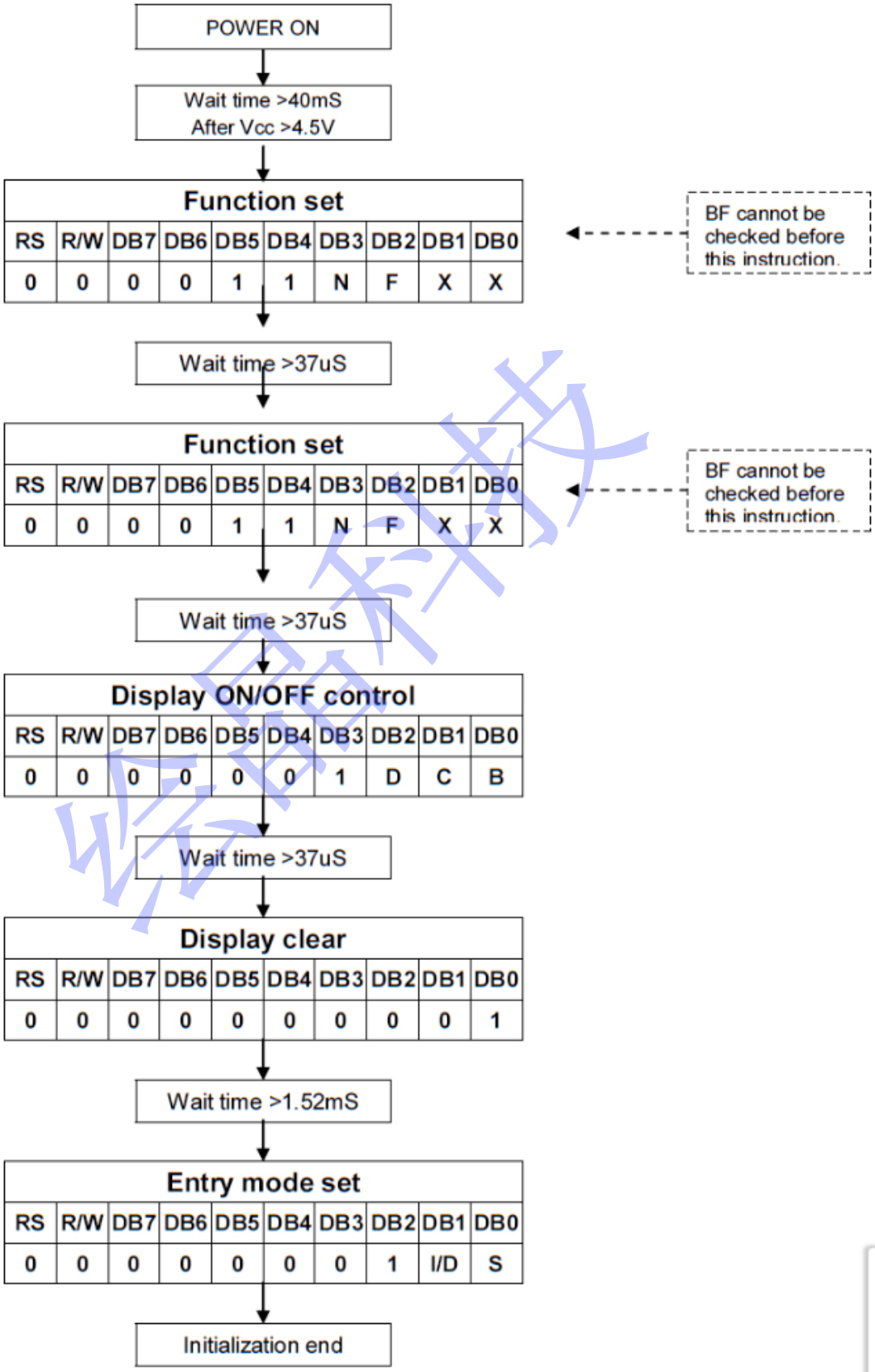
8.MPU Connection diagram




INPUT
VDD
+C_VDD
22uF
C51 MCU
mcu
P0.0/AD0
P0.1/AD1
P0.2/AD2
P0.3/AD3
P0.4/AD4
P0.5/AD5
P0.6/AD6
P0.7/AD7
P2.0/A8
P2.1/A9
P2.2/A10
P2.3/A11
P2.4/A12
P2.5/A13
P2.6/A14
P2.7/A15
CLED
P10
P11
P12
P13
P14
P15
P16
P17
P3.0/RXD
P3.1/TXD
P3.2/INT0
P3.3/INT1
P3.4/T0
P3.5/T1
P3.6/WR
P3.7/RD
A0
WR
E
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
MCU_STOP
R_RST
10K
CY1
20pF
Y1
12M
XTAL1
XTAL2
ALE/PROG
PSEN
EA/VPP
RST
VCC
VSS
89S52
MCU_RST
C_RST
1uF
RV
10K
V0
LCD
VSS
VDD
V0
RS
R/W
E
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
LEDA
LEDK
CON16_
Q?
MOSFET N
Title
Size
A
Number
Revision
Date:
4-Jul-2020
Sheet of
File:
Drawn By:

9.Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.



10. Reference drive source code

```
#include<reg52.h>
#include <intrins.h>
sbit RS=P3^1;//
sbit RW=P3^4; //
sbit E=P3^5;  //
sbit stop=P3^2;//
//DB7-DB0 : P1

typedef unsigned int uint;
typedef unsigned char uchar;
unsigned char command,LCDdata,j;
unsigned int m,i,k;
uchar code CGRAM[];
uchar code table[]= "YEIYEI";
uchar code table1[]="01234567";
uchar code table2[]="TIME";
uchar num,ii,z,z1,d,d1,s,s1,s10,s100;


void WaitNms(unsigned int x)// x ms
{
unsigned char j;
while(x--)
{for(j=0;j<125;j++)
{;}
 }
}

void WaitNus(unsigned int x)// x us
{
unsigned char j;
while(x--)
{for(j=0;j<12;j++)
{;}
 }
}


 void INTI () interrupt 0 using 1

{
 for(;;);
```

40ms

```
}


void BUSYFLAG(void)
{
uchar temp;
P1=0xff;
RS=0;
RW=1;
    while(1)
  {
    E=1;
    temp=P1;                    //
    E=0;
    if ((temp&0x80)==0)
    break;                    //
  }
}

void writeCommand(uchar command)
{
BUSYFLAG();
RS=0;
RW=0;

E=1;
P1=command;
E=0;
}
void writeData(uchar DATA)
{
BUSYFLAG();
RS=1;
RW=0;

E=1;
P1=DATA;
E=0;
}


LCDINT(void)
{
WaitNms(15);//// x ms
```

```
writeCommand(0x30);//8位
WaitNms(4);//// x ms
writeCommand(0x30);
WaitNus(100);//// x us
writeCommand(0x30);

writeCommand(0x38);//
writeCommand(0x01);//
writeCommand(0x06);//
writeCommand(0x0c);//
writeCommand(0x80);//
}

void storeCGRAM(uchar d1,uchar d2)
    {
        for(i=0;i<4;i++)
             {
              writeData(d1);
              writeData(d2);
             }
     }


void writetest(uchar dd)
    {
        for(i=0;i<80;i++)
          {
           writeData(dd);
          }
    }


void writeALLcharacter(void)
{
for(i=0x20;i<(0x20+80);i++)//写ASCLL码
  {
 writeData(i);
  }
 WaitNms(500);////延时 x ms
writeCommand(0x01);//清屏
for(i=0xC0;i<(0xC0+80);i++)//写ASCLL码
  {
 writeData(i);
  }
```

```
}


main(void)//////////////////////////////////
{
uchar m1;
//-------------------------------------//
for(m1=0;m1<20;m1++)
    {

      EA=1;
      EX0=1;
      IT0=1;

    LCDINT();

    writeCommand(0x40);       //
    storeCGRAM(0xff,0xff);
    storeCGRAM(0xff,0x00);
    storeCGRAM(0x00,0xFF);
    storeCGRAM(0xAA,0xAA);
    storeCGRAM(0x55,0x55);
    storeCGRAM(0xAA,0x55);
    storeCGRAM(0x55,0xAA);

    writeCommand(0x80);
    for(ii=0;ii<7;ii++)
        {
        writetest(ii);//LCD
        WaitNms(350);//// x ms
        }
    writeCommand(0x01);//

    writeALLcharacter();//
    WaitNms(400);//// x ms
    writeCommand(0x01);//

    writeCommand(0x80+5);//
    for(num=0;num<7;num++)
        {
            writeData(table[num]);
            WaitNms(100);//// x ms
        }
        WaitNms(100);////延时 x ms
```

```
        writeCommand(0x80+(0x40+5));//
    for(num=0;num<6;num++)
        {
            writeData(table1[num]);
            WaitNms(100);//// x ms
        }
        WaitNms(400);//// x ms
    }

//-----------------------------------------//

        writeCommand(0x01);//
        writeCommand(0x80);//
    for(num=0;num<7;num++)
        {
            writeData(table[num]);
            WaitNms(100);//// x ms
        }
        WaitNms(100);//// x ms
        writeCommand(0x80+8);//
    for(num=0;num<8;num++)
        {
            writeData(table1[num]);
            WaitNms(100);//// x ms
        }
        writeCommand(0x80+0x40);//
    for(num=0;num<4;num++)
        {
            writeData(table2[num]);
            WaitNms(100);//// x ms
        }

//-------------------------------------
    writeCommand(0x80+(0x40+7));//
    writeData(0x3a);

    for(z=0;z<10;z++)

    {
        writeCommand(0x80+(0x40+5));//
        writeData(0x30+z);   //
        for(z1=0;z1<10;z1++)

        {
```

```
        writeCommand(0x80+(0x40+6));//
        writeData(0x30+z1);  //
        for(d=0;d<6;d++)
        {

            writeCommand(0x80+(0x40+8));//
            writeData(0x30+d);   //
            for(d1=0;d1<10;d1++)
            {
                writeCommand(0x80+(0x40+9));//
                writeData(0x30+d1);  //

                for(s=0;s<6;s++)
                {

                    writeCommand(0x80+(0x40+10));//
                    writeData(0x3a);
                    writeCommand(0x80+(0x40+11));//
                    writeData(0x30+s);   //

                    for(s1=0;s1<10;s1++)
                    {
                        writeCommand(0x80+(0x40+12));//
                        writeData(0x30+s1);      //
                        WaitNms(10);////延时 x ms
                        writeCommand(0x80+(0x40+13));//
                        writeData(0x3a);
                        for(s10=0;s10<10;s10++)
                        {
                            writeCommand(0x80+(0x40+14));//
                            writeData(0x30+s10);//100MS
                            WaitNms(10);////延时 x ms
                            for(s100=0;s100<10;s100++)
                            {
                            writeCommand(0x80+(0x40+15));//
                            writeData(0x30+s100);//10MS
                            WaitNms(10);////延时 x ms
                            }
                        }
                    }
                }
            }
        }
    }
```

```
    }
}


//----------------------------end----------------------------
```

DOCUMENT REVISION HISTORY

VERSION	DATE	DESCRIPTION	CHANGED BY
V1	2023 03 29	First issue	YXS
V2	2023 04 19	Change ST7066 or EQV to ST7066U/ 按客户要求 ST7066 or EQV 改为 ST7066U	YXS
V3	2023 04 20	Annotate sequence diagram as required by customer/客户要求标注时序图	YXS
V4	2023 05 05	Update AC Characteristics	YXS
V5	2023 05 05	按客户强制改错波形图	YXS
V6	2023 05 23	Modify as required by customer	YXS
V7	2023 08 31	Modify as required by customer	YXS
V8	2023 11 09	R6 电阻由 220R 改 820R(注 R6 电阻非决定值)/ R6 resistance changed from 220R to 820R (Note The R6 resistance is non-deterministic)	YXS
V9	2024 01 18	按实际测量 VLCD、IDD 标示/ According to the actual measurement VLCD, IDD mark	YXS